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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,726	10/24/2001	Kenneth Y. Ogami	CYPR-CD01171M	2851
7590 06/10/2005 WAGNER, MURABITO & HAO LLP Two North Market Street, Third Floor San Jose, CA 95113			EXAMINER SIEK, VUTHE	
			ART UNIT 2825	PAPER NUMBER

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,726	OGAMI ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11, 13-17 and 19-37 is/are rejected.
- 7) ☒ Claim(s) 12 and 18 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to application 10/002,726 and communications filed on 3/21/2005. Claims 1-37 remain pending in the application and claims 38-41 are have been canceled as to non-elected claims.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 4-10, 22-23, 25-31 and 33-37 are rejected under 35 U.S.C. 102(a/e) as being anticipated by Barnett et al. (6,223,144).

4. As to claims 1, 22 and 30, Barnett et al. teach a microcontroller software tool for selecting available hardware configurations of hardware resources of a microcontroller for producing a modular configuration of selected hardware configurations and software development environments of a microcontroller by accessing a description of hardware resources of the microcontroller (Figs. 1B and 2 and its description; col. 5-6). Barnett et al. teach that the microcontroller software testing tool comprises of a configuration core (configuration core of a microcontroller), and additional Dynamic Link Libraries that

Art Unit: 2825

interface the tool to selected hardware configurations (selected hardware configurations of microcontrollers or selected configurations of dynamically configurable blocks to produce a variety of functions). This would explicitly imply that Barnett et al. teach configuring a microcontroller including generating configuration information corresponding to a selected configuration.

5. As to claims 2, 23 and 31, Barnett et al. teach the description of the hardware resources comprising a text readable data structure (col. 5-6).

6. As to claims 4-5, 25-26 and 33-34, Barnett et al. teach selected configurations and software development environments to prove a modular configuration (col. 5-6) (predetermined configurations that are user modules to produce the selected configuration).

7. As to claims 6, 27 and 35, Barnett et al. teach the DLL contains all microcontroller specific information (instruction set) and hardware characteristic to configure a microcontroller (col. 6).

8. As to claim 7-8, 28-29 and 36-37, Barnett et al. teach application programming interface calls for embedded software (col. 5), wherein the application programming interface calls are named according to names given to configurations of the hardware resources (Figs. 2B-2D).

9. As to claim 9, Barnett et al. teach generating an interrupt vector table for use by embedded software, wherein a plurality of interrupts in the interrupt vector table are generated by the selected configuration (Fig. 2C).

Art Unit: 2825

10. As to claim 10, Barnett et al. teach using microcontroller software testing tool for tracking the selected configuration (tracking the selected configuration and informing user) (col. 5-6) and informing a user if the selected configuration is achievable using the hardware resources is inherently included within the process. Claims 1-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Snyder (6,825,689).

11. The applied reference below (Snyder) has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

12. As to claims 1, 11, 22 and 30, Snyder teaches a microcontroller device comprising a configurable interface consisting of input/output (I/O) pin, configuration system, global mapping system, and a microprocessor to generate a configuration information corresponding to a selected configuration of hardware resources of a microcontroller. The configuration system can, depending upon its configuration, selectively couple I/O pin with either a microprocessor or global mapping system. The mapping system is coupled with a plurality of functional units of digital configuration system macro (DCSM). The global mapping system selectively couples I/O pin with a selected functional unit or units of DCSM, where the functional units of DCSM are programmable digital and analog units which can be configured and connected by a

Art Unit: 2825

user as needed to create a customized microcontroller device (dynamic functional units). The global mapping system is maintained by a control program which supplies the logic to selectively couple I/O pin with functional units of DCSM. The present invention provides a configurable I/O interface for a microcontroller which allows, a designer a greater flexibility to easily create customized configurations (configuration information), and requires no unusual design skills. The present invention also allows a microcontroller device to be reconfigured dynamically without being limited by pin configuration. The present invention further allows selectively coupling an I/O pin to a microprocessor device and to reconfigure this coupling per clock cycle. The interface between the I/O pin and the rest of system can be dynamically configured by software created or modified by a user, or by hardware (see abstract, summary, Fig. 1-4 and its description, col. 3, lines 64-67, col. 4, lines 1-67; col. 5, lines 1-67, col. 6, lines 1-46).

13. As to claims 2, 4-8, 10, 13-18, 19-21, 23, 25-29, 31, and 33-37, Snyder teaches a microcontroller device comprising a configurable interface consisting of input/output (I/O) pin, configuration system, global mapping system, and a microprocessor to generate a configuration information corresponding to a selected configuration of hardware resources of a microcontroller. The configuration system can, depending upon its configuration, selectively couple I/O pin with either a microprocessor or global mapping system. The mapping system is coupled with a plurality of functional units of digital configuration system macro (DCSM). The global mapping system selectively couples I/O pin with a selected functional unit or units of DCSM, where the functional units of DCSM are programmable digital and analog units (user modules) which can be

Art Unit: 2825

configured and connected by a user as needed to create a customized microcontroller device (dynamic functional units). The global mapping system is maintained by a control program which supplies the logic to selectively couple I/O pin with functional units of DCSM. The present invention provides a configurable I/O interface for a microcontroller which allows (application programming interface), a designer a greater flexibility to easily create customized configurations (configuration information), and requires no unusual design skills. The present invention also allows a microcontroller device to be reconfigured dynamically without being limited by pin configuration. The present invention further allows selectively coupling an I/O pin to a microprocessor device and to reconfigure this coupling per clock cycle. The interface between the I/O pin and the rest of system can be dynamically configured by software created or modified by a user, or by hardware (hardware resources) (see abstract, summary, Fig. 1-4 and its description, col. 3, lines 64-67, col. 4, lines 1-67; col. 5, lines 1-67, col. 6, lines 1-46).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claims 3, 24 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barnett et al. (6,223,144) in view of Zizzo (6,578,174).

16. As to claims 3, 24 and 32, Barnett et al. does not explicitly teach the text readable data structure is substantially compliant with extensible markup language (XML). Zizzo teaches a method and system for chip design using remotely located resources comprising circuit design platform to facilitate the design of an IC by making it easier for designers to locate and incorporate available virtual component blocks into new designs include using a universal data interface format or mark-up language (XML) is preferably used as a primary data interface between the various components of the system and the details XML are well-known to those in the art of computer programming (col. 7, 9). Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to implement the description of hardware resources with extensible markup language (XML) because its universal data format, the XML language would be easy to implement and preferably used as primary data interface between various components (EDAs) of the design platform.

Remarks

17. Applicant(s) argued that Barnett et al. do not teach or suggest selecting available configurations of the hardware resources of said microcontroller. Examiner respectfully submits that Barnett teach providing the microcontroller software testing tool comprises a configurable core (configurable microcontroller), additional dynamic link libraries (DDLs) 210 and 220 (corresponding to configurable core of a microcontroller) that interface the microcontroller software testing tool to selected hardware configurations (selected available configurations of the hardware resources of said microcontroller)

Art Unit: 2825

and software development environments respectively to provide a modular microcontroller (generating configuration information corresponding to the selected configuration) (col. 6, lines 6-13): In this manner, the microcontroller software testing tool can support any microcontroller or any code development suite. Also, applicant(s) argued that a combination of Barnett and Zizzo is not proper. Barnett teaches the microcontroller software tool to be accessed over Internet. In this manner, the general purpose controlling programs can load, run, and interrogate the microcontroller software tool and record results in a standard document. Zizzo teaches a method and system for chip design using remotely located resources, where a universal data interface format or mark-up language (XML) is preferably used as a primary data interface between the various components of the system. The detailed of XML are well-known to those in the art of computer programming. Therefore, it would have obvious to one of ordinary skill in the art at the time the invention was made to implement the description of hardware resources with extensible markup language (XML) because its universal data format, the XML language would be easy to implement and preferably used as primary data interface between various components (EDAs) of the design platform, thereby facilitating configuring the microcontroller.

Allowable Subject Matter

1. Claims 12 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek


VUTHE SIEK
PRIMARY EXAMINER